For a square or narrow gap ($d \ll 2D + l$), two-dimensional approximation is irrelevant. Our results for finite-thickness conductors are shown in Fig. 2, where $t_0 = 0.1\ \mu$m, $d_0 = 0.15\ \mu$m, $t_1 = 0.2\ \mu$m, $\lambda = 0.09\ \mu$m, and $l = 5$, $D = l/2$, $2w + d = 4l$. The values of L_{22} and L do not converge to the inductance of the strip without a hole because the current in ground plane needs to flow around the cut.

VIII. Conclusions

In this paper, we have proposed a new numerical technique for analyzing planar multilayer superconductor circuits. The developed program allows us to calculate inductances for realistic 3-D circuits yielding very reasonable CPU time.

Our program can be applied for calculation of inductances of perfect conductors simply setting to zero the London penetration depth.

The results of this paper can be extended to the case of impedance calculation of normal conductors.

The program can be implemented as a component in electromagnetic computer-aided design (CAD) complexes.

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A Design of the Ceramic Chip Balun Using the Multilayer Configuration

Dae-won Lew, Jun-Seok Park, Dal Ahn, Nam-Kee Kang, Chan Sei Yoo, and Jae-Bong Lim

***Abstract*—This paper presents the design method and performance characteristics of a chip-type balun using a multilayer structure. The design method for a chip-type balun is based on the lumped-element equivalent circuit of quarter-wave transformer. The proposed design method and equivalent circuit can make it easy to design the ceramic multilayer chip-type balun. The size 2012 and 3216 chip-type baluns were designed and fabricated using the proposed design method and the equivalent-circuit model of a quarter-wave transformer. Fabrications and measurements of designed chip-type baluns show smaller size than conventional chip-type baluns and good agreement with simulated results.**

***Index Terms*—Multilayer structure, quarter-wave transformer, 2012 and 3216 chip-type balun.**

I. Introduction

Multilayer configurations can provide several advantages in the integration and compaction of RF and microwave components, circuits, and systems. Another reason for employing the multilayer configurations is that several circuits function such as baluns, coupler, etc., which are difficult to realize in a single-layer planar configuration, can be obtained conveniently in two- or multiple-layer configurations. Several kinds of multilayer passive components, such as filters, couplers, and balun, have been developed and each design methods and fabrication procedures have been reported. The baluns and couplers require no suspended substrate techniques. Hence, they can be easily incorporated in the design of a variety of components such as mixers, multipliers, and push–pull class-B amplifiers [1]–[4].

In this paper, an approach for the design of a chip-type balun using a multilayer structure is presented. The presented design method for the chip-type balun is developed using the equivalent circuit of a quarter-wavelength transformer. By employing the proposed design method and equivalent-circuit model, the designed multilayer chip balun configuration can be made more compact and flexible, providing better performances. The designed chip-type balun was realized by implementing the multilayer chip inductors and capacitors. Each lumped element was implemented using the ceramic material and Ag metal layers. The dielectric constant was chosen to be six for the implementation.

This paper presents the experimental results showing the changing of the frequency characteristics with a lumped-element value. Simulation results and experimental measurements for the designed chip-type balun show a validation of the proposed design method.

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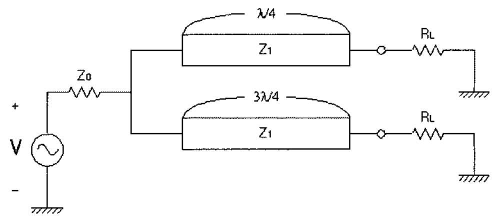


Fig. 1. Equivalent transmission-line representation of the balun with $\lambda/4$ and $3\lambda/4$ transformers.

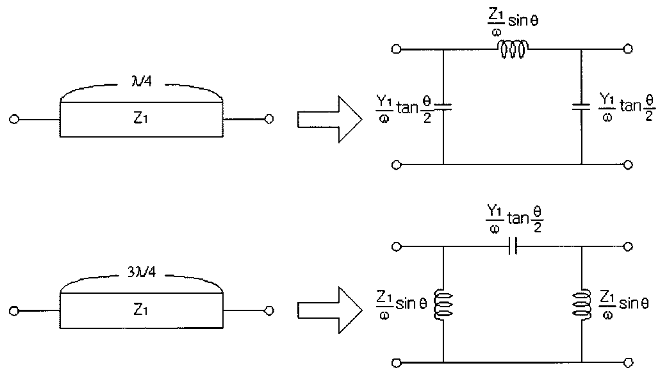


Fig. 2. π-type equivalent-circuit representation and equivalent parameters for each quarter-wavelength transformers.

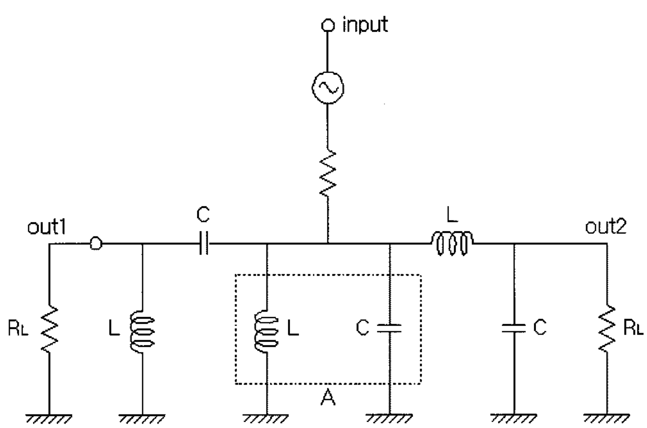


Fig. 3. Lumped equivalent circuit for the balun using π-type equivalent-circuit representation for each quarter-wavelength transformers.

II. Design Procedure

The quarter-wave transformer is a useful and practical circuit for impedance matching [5]. Fig. 1 shows the equivalent transmission-line representation of the balun [6]. Each balance port is connected $\lambda/4$ and $3\lambda/4$ transformers in order to simultaneously accomplish matching and out-of phase conditions.

Characteristic impedance Z_1 of the quarter-wavelength transformer is expressed as follows [7]:

$$Z_1 = \sqrt{2Z_0 \cdot R_L}. \tag{1}$$

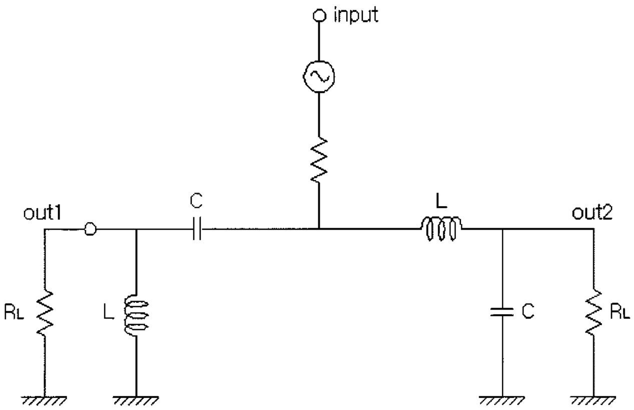


Fig. 4. Final equivalent circuit for the balun, which is corresponding to a conventional lead–lag circuit.

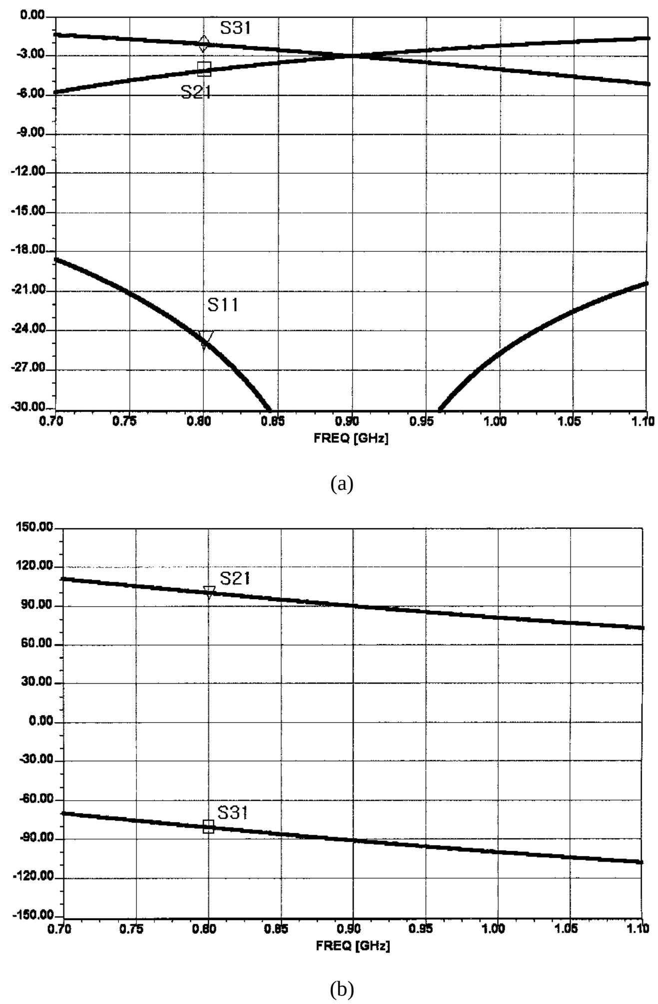
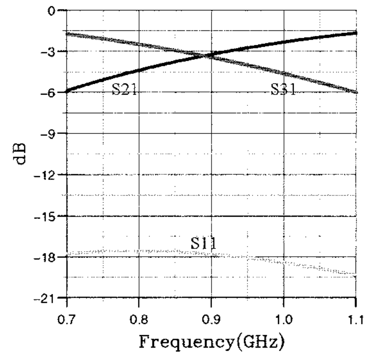
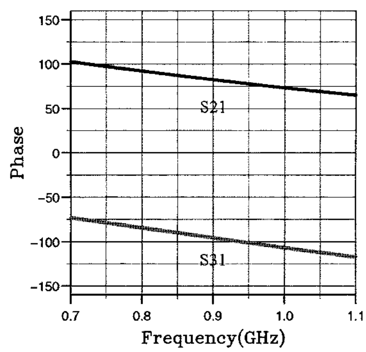


Fig. 5. Simulated results of designed 3216 chip balun based on the equivalent circuit using an Ansoft circuit simulator. (a) Magnitude characteristic. (b) Phase characteristic.

Each quarter-wavelength transformer can be represented to a π-type equivalent circuit using even-odd mode analysis, as shown in Fig. 2. Thus, by employing the π-type equivalent circuits of each quarter-



(a)



(b)

Fig. 6. Simulated results of designed 3216 chip balun by HFSS. (a) Magnitude characteristics. (b) Phase characteristic.

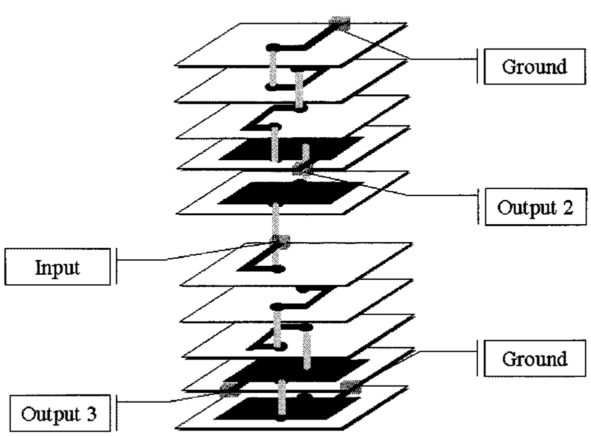
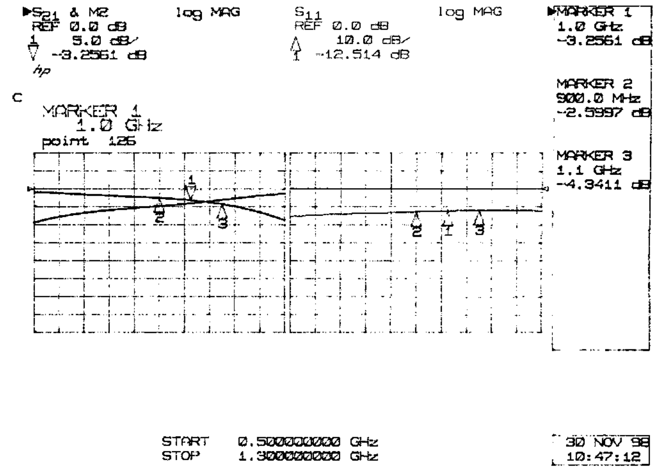
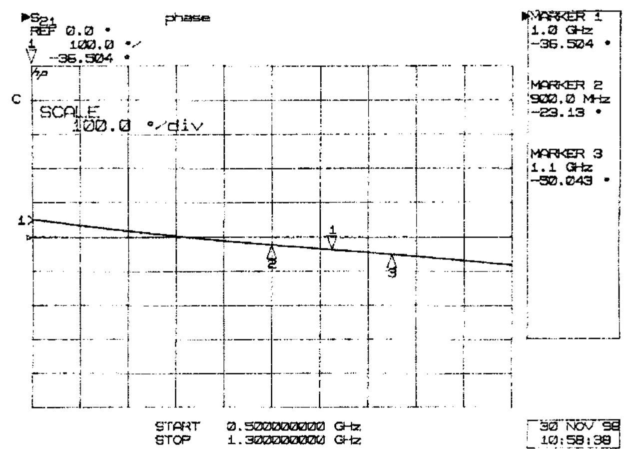


Fig. 7. Layer configuration of the chip-type balun. The dielectric constant of ceramic sheet is 6.0. The thickness of the ceramic and metal layers was kept at 60 and 30 μm, respectively. The physical overall size are 3.2 mm × 1.6 mm × 1.1 mm and 2.0 mm × 1.2 mm × 1.1 mm, which are corresponding to sizes 3216 and 2012, respectively.



(a)



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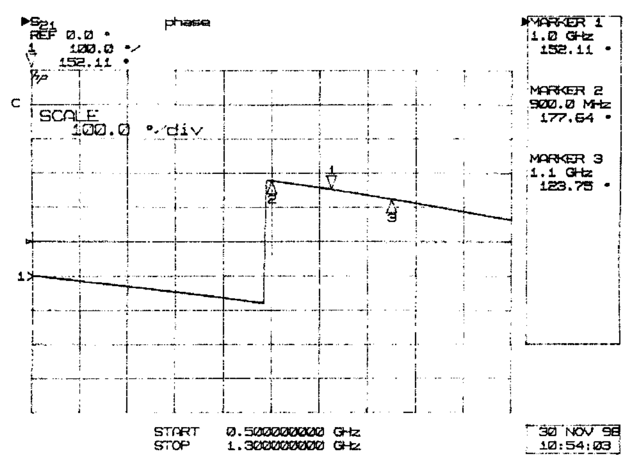

(c)

Fig. 8. Measured results of the fabricated 3216 ceramic chip balun. (a) Insertion- and return-loss characteristic. (b) Phase characteristic of S_{21}. (c) Phase characteristic of S_{31}.

wavelength transformer, the equivalent circuit of the balun can be represented as shown in Fig. 3 [8], [9].

Parallel resonator in Fig. 3, which is boxed with a dashed line, can be omitted since the susceptance of a parallel LC resonator is zero at the center frequency of the balun. The final equivalent circuit consists of lead and lag lumped circuits, as shown in Fig. 4. These lead and lag lumped circuits produce the out-of-phase characteristic at both output ports.

The equivalent-circuit element value can be derived as follows:

$$L = \frac{Z_1}{\omega_o} \sin\theta \tag{2}$$

$$C = \frac{Y_1}{\omega_o} \tan\frac{\theta}{2} \tag{3}$$

where ω_o is the center angular frequency of the designed balun and Y_1 means $1/Z_1$.

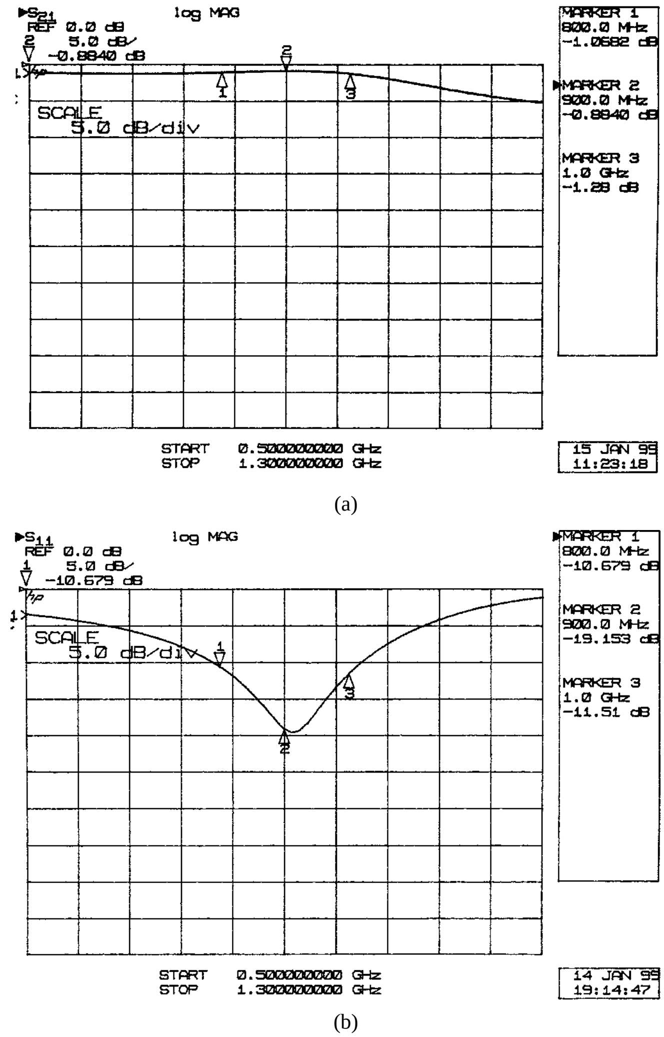

Fig. 9. Measured results of the fabricated 2012 ceramic chip balun. (a) Insertion-loss characteristics for a back-to-back type. (b) Return-loss characteristics for 400-Ω termination case.

TABLE I
FREQUENCY CHARACTERISTIC WITH DIFFERENT CAPACITANCES

Sample No.	L (nH)	C (pF)	Center frequency (MHz)
1	12.5	6.14	784
2	12.5	4.65	900
3	12.5	3.64	1072

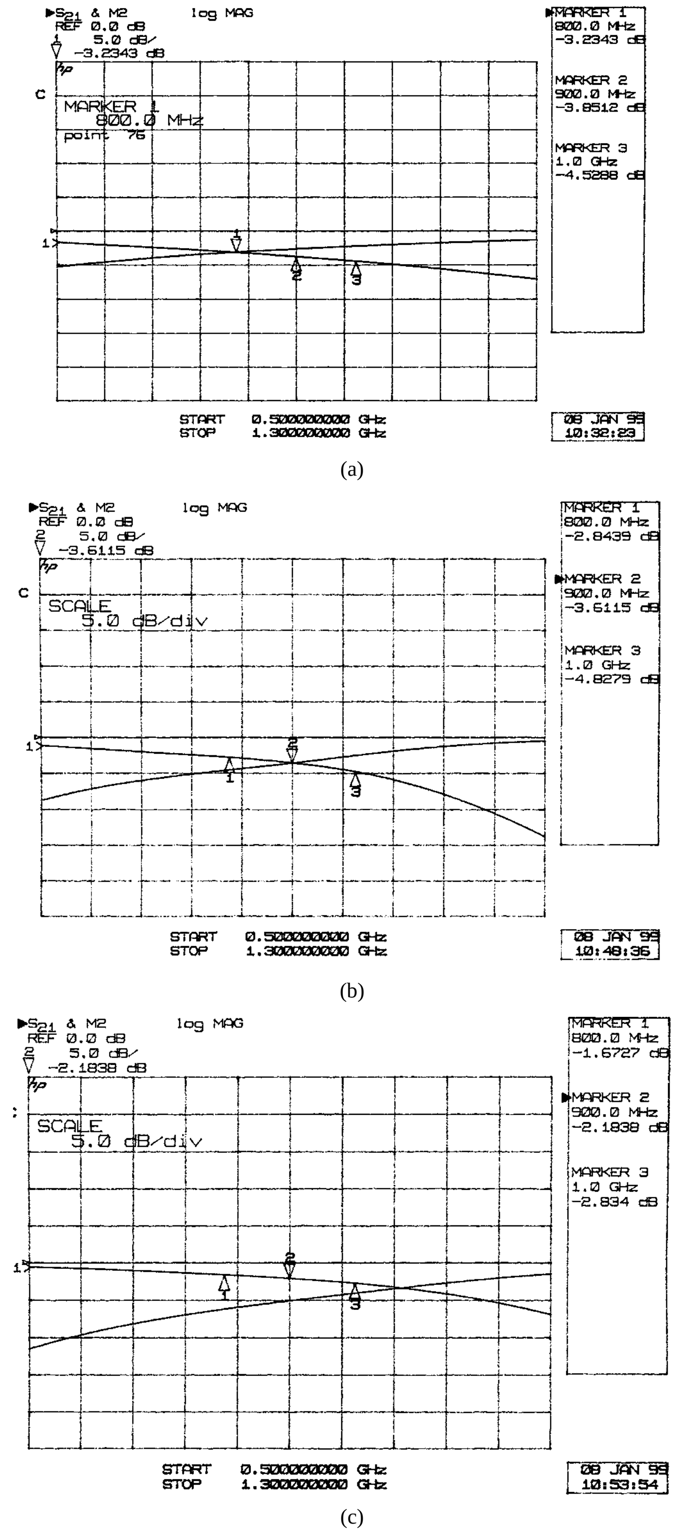

Fig. 10. Frequency characteristic of fabricated chip baluns with different capacitances. (a) $C = 6.14$ pF. (b) $C = 4.65$ pF. (c) $C = 3.64$ pF.

III. DESIGN AND SIMULATION

The size 3216 and 2012 chip-type baluns were designed by using proposed equivalent circuit and design method with the operating frequency range of 800–1000 MHz. Each unbalanced port impedance were chosen to be 50 Ω : 50 Ω and 50 Ω : 200 Ω, respectively. The designed chip type balun was simulated with Serenade and HFSS, which are part of Ansoft's software package. Fig. 5 show the simulation results of the designed 3216 chip balun based on the equivalent circuit. The simulated results for designed 3216 chip balun by HFSS are shown in Fig. 6. As shown in Fig. 6, the insertion and return losses are less than -1.0 and -17 dB in the operating frequency range, respectively. The difference between balance ports is less than 2 dB. The phase difference between balance ports is 180° with ±1% tolerance over the operating frequency range.

IV. Fabrication and Experimental Results

Fig. 7 shows the layer configuration of the fabricated chip-type balun. The designed chip-type baluns were fabricated with a multilayer configuration using ceramic sheets, which has a dielectric constant of 6.0 and a thickness of 60 μm, and Ag metal pattern. The thickness of the metal layer was kept at 30 μm. The physical overall size are 3.2 mm $\times$ 1.6 mm $\times$ 1.1 mm and 2.0 mm $\times$ 1.2 mm $\times$ 1.1 mm, which are sizes 3216 and 2012, respectively. There must be parasitic couplings between the fabricated inductor and capacitor. In order to resolve this parasitic coupling effects, each inductor and capacitor are separated using the ceramic isolation layers which are 100-μm thick.

Figs. 8 and 9 show the experimental results of the fabricated 3216 chip balun with $50\,\Omega : 50\,\Omega$ unbalanced ports termination and the fabricated 2012 chip balun with $50\,\Omega : 200\,\Omega$ unbalanced ports termination. The insertion and return losses are less than -1.3 and -10 dB over the operating frequency band, respectively. The measured phase characteristics between balance ports of the 3216 chip balun show the difference of 180° with ±3% tolerance over the operating frequency range.

There must be some deviations of characteristics, such as the operation frequency, in fabricated baluns due to the multilayer process tolerance. In order to show the variation of the frequency characteristics for the designed chip balun dependent on the lumped-element value, three kinds of chip baluns, which have different capacitance, were designed and fabricated. Table I and Fig. 10 show the experimental results for the three kinds of chip baluns with different capacitance. Decreasing the capacitance increases the resonance frequency of the parallel *LC* circuit and the impedance. Thus, it increases the operating frequency.

V. Conclusions

The design method and equivalent circuit of the chip-type balun have been proposed in this paper to provide a simple design procedure, compact size, and excellent performance. Two kinds of chip-type baluns were designed based on the proposed equivalent model with the equivalent-circuit representation of the quarter-wavelength transformer and fabricated with a multilayer ceramic process. The proposed design method for chip-type balun is entirely based on a lumped-element equivalent circuit. Thus, the derived equivalent circuit could provide a quite simple and accurate design equation. Furthermore, the variation of the operating frequency with the changing of the lumped-element value has been discussed in order to investigate the deviation of the frequency characteristic in a fabricated chip-type balun. The presented equivalent-circuit model and design method of the multilayer chip balun can offer smaller efforts in designing multilayer chip baluns.

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A Suitable Integral Equation for the Quasi-TEM Analysis of Hybrid Strip/Slot-Like Structures

Jesús Martel and Francisco Medina

***Abstract*—This paper reports on a suitable formulation of the spectral-domain/integral-equation method for the quasi-TEM analysis of hybrid strip/slot-like planar lines. The free surface charge distribution is used as an unknown on the strip-like interface, whereas the electric field is used on the slot-like region. This formulation allows us to reduce the number of basis functions and makes possible a unified treatment of the problem. A single type of basis functions is used, leading to a quasi-analytical evaluation of the Galerkin matrix entries. The performance of the method is illustrated with a practical example structure useful for coupler design.**

***Index Terms*—Galerkin method, quasi-TEM analysis, strip/slot-like structures.**

I. Introduction

Planar multiconductor lines are widely used in microwave and millimeter-wave circuits. Although full-wave methods are available for the analysis of this type of transmission structures, quasi-static approaches are still useful for computer-aided design (CAD) purposes because they yield very fast codes still accurate enough for preliminary designs. Most of these transmission systems can be classified either as strip- or slot-like. The former can be described as a number of coupled conducting strips embedded in a layered medium, whereas the latter are best described as a number of slots practiced in a grounded metallization. The quasi-static analysis of structures of both categories has been carried out by means of a variety of techniques. In particular, integral-equation formulations (both in the spectral and spatial domain) making use of suitable basis functions and quasi-analytical techniques to evaluate numerical series or integrals have proven to be both fast and versatile in the analysis of strip-like [1]–[3] and slot-like [4], [5] structures. For strip-like structures, the integral equation should be formulated for the free surface charge distribution on the strips, while for slot-like ones, the problem is better posed in terms of the slots electric field. The per unit length (p.u.l.) capacitance matrix $[C]$ or its inverse $[P]$ are directly obtained from the solution of the above-mentioned integral equations. However, more complicated geometries in-

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